

PATENT ABSTRACTS OF JAPAN

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(54) SAMPLING FREQUENCY CONVERTER

(57)Abstract:

PURPOSE: To cope with even the asynchronous timing of an input/ output sampling frequency by performing conversion between arbitrary sampling frequencies with one filter coefficient.

CONSTITUTION: This converter is provided with a storage means 101 where a certain number of input digital signals having a first sampling frequency are held and a digital low pass filter (FIR filter) 102 which takes out input digital signals from the position, which is determined by the input/output sampling frequency ratio of the storage means 101, by the tap length and multiplies the first sampling frequency by (n) ((n) is a certain fixed value) to perform interpolation. Further, a linear interpolation means 103 which improves the accuracy of an output digital signal sample value having a second sampling frequency is provided. The input digital signal is inputted at the timing of the first sampling frequency, and the output digital signal is outputted at the timing of the second sampling frequency, and conversion between arbitrary input/output sampling frequencies is performed. A means which updates the input/output sampling frequency ratio is added to realize asynchronous coupling.

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CLAIMS

[Claim(s)]

[Claim 1] A storage means to hold a fixed number of input digital signals which have the 1st sampling frequency, n time-izing [an input digital signal is taken out from the location determined by the I/O sampling-frequency ratio of said storage means by tap length, and / the 1st sampling frequency] interpolation (n is a certain fixed value) The digital low pass filter to carry out, It has the linear interpolation means which raises the accuracy of the output digital signal sampled value which has the 2nd sampling frequency. The sampling-frequency inverter which inputs an input digital signal to the timing of the 1st sampling frequency, outputs an output digital signal to the timing of the 2nd sampling frequency, and performs conversion between the I/O sampling frequencies of arbitration.

[Claim 2] The sampling-frequency inverter [equipped with a means to update an I/O sampling-frequency ratio in order to enable asynchronous association] according to claim 1.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to the sampling-frequency inverter for

changing the input digital signal which has the 1st sampling frequency into the output digital signal which has the 2nd sampling frequency.

[0002]

[Description of the Prior Art] The sampling frequency F_s when sampling analog signals, such as an audio signal, and changing into a digital signal changes with use media. For example, in the sampling frequency of 44.1kHz and a satellite broadcasting service A mode sound signal, the sampling frequency of 32kHz and this B mode sound signal is [the sampling frequency of the sound signal corresponding to TV signal of NTSC system / the sampling frequency of 44.056kHz and CD] 48kHz.

[0003] A sampling frequency must be changed when carrying out interconnect between the media from which these sampling frequencies differ generally.

[0004] the configuration of the sampling-frequency inverter of the former [drawing 5] -- being shown -- **** -- M/N -- the approach called law is used. In drawing 5, it increases the over sampling technique of the input digital signal which has the 1st sampling frequency inputted into the over sampling technique filter 501 N times, and it serves as an input of the following infanticide means 502. Here, N is the integral value beforehand calculated by the degree type (1). The digital signal inputted into the infanticide means 502 is also changed into the output digital signal which are-izing [a digital signal / the integer M similarly searched for by the degree type (1) / $1/M$ time], and has the 2nd sampling frequency for it.

[0005] $M: N = F_{s1} : F_{s2} \dots\dots\dots (1)$

However, for the input sampling frequency F_{s2} , the output sampling frequencies M and N are [F_{s1}] an integer [0006]. Thus, conversion to the 2nd sampling frequency from the 1st sampling frequency can be carried out also with the above-mentioned conventional sampling-frequency inverter.

[0007]

[Problem(s) to be Solved by the Invention] However, since it existed by the combination of the 1st and 2nd sampling frequencies and only the number corresponding to it needed to prepare a filter factor, the conversion between the sampling frequencies of arbitration was impossible for the degree N of the over sampling technique filter [in / since a sampling frequency when over sampling technique is carried out turns into the least common multiple of the 1st and 2nd sampling frequencies in the above-mentioned conventional sampling-frequency inverter / drawing 5] 501 as a matter of fact.

[0008] This invention solves such a conventional problem, enables conversion between the sampling frequencies of arbitration by one filter factor, and aims at offering the outstanding sampling-frequency inverter which can respond also when the timing of an I/O sampling frequency is asynchronous.

[0009]

[Means for Solving the Problem] a means to memorize an input digital signal in order that this invention may attain the above-mentioned purpose, and the input digital

signal which has the 1st sampling frequency -- n -- it has the digital low pass filter which and is interpolated, and the linear interpolation means which raises the accuracy of the output digital signal sampled value which has the 2nd sampling frequency. [a low pass filter] [a low pass filter] [time]

[0010]

[Function] Therefore, according to this invention, by carrying out the infanticide by the linear interpolation means, even if it fixes the multiplier of the digital low pass filter of the preceding paragraph to one, an output digital signal can be searched for with a sufficient precision, and it has the effectiveness that conversion between the sampling frequencies of arbitration can be performed. By having a means to memorize an input digital signal furthermore, it has the effectiveness that it can respond also when the timing of an I/O sampling frequency is asynchronous.

[0011]

[Example] Drawing 1 shows the configuration of the 1st example of this invention. In drawing 1, 101 is an input digital signal storage means, and 102 is an FIR filter as a digital low pass filter for restricting the band more than the Nyquist rate of the sampling frequency of the smaller one among I/O at the same time it interpolates an input digital signal n times. 103 is a linear interpolation means for raising and thinning out the accuracy of the 2nd digital signal sampled value.

[0012] Next, actuation of the 1st example of the above is explained. In the above-mentioned example, an input digital signal is stored in the input digital signal storage means 101 to the timing of the 1st sampling frequency. The input digital signal storage means 101 holds many numbers of sampled value using a ring buffer like drawing 3 rather than the number of taps required for the operation of the FIR filter 102 of the next step.

[0013] The input digital signal sample stored in the input digital signal storage means 101 is read from the suitable location of the input digital signal storage means 101 only several tap minutes required for the operation of the FIR filter 102 of the next step, and is inputted into the FIR filter 102. The suitable location of the input digital signal storage means 101 at this time sets the location of the first output side pointer (it expresses as a drawing solid line) to the diagonal location of an input-side pointer, as shown in drawing 3, and the location (it expresses as a drawing destructive line) of the output side pointer from a degree is determined by moving by the I/O sampling-frequency ratio of the degree type (2) for which it asked beforehand.

[0014] $\text{Tau} = F_s \cdot 1 / F_{s2} \dots\dots\dots (2)$

However, tau is an I/O sampling-frequency ratio [0015]. On the other hand, the FIR filter 102 interpolates an input digital signal sample train to one n times the fixed value like a degree type (3) of this.

[0016]

$n = 256 \dots\dots\dots$ It is $\text{INT} (256 / \text{tau})$ at the time of $F_{s1} \leq F_{s2} \dots$ At the time of $F_{s1} > F_{s2} \dots$
(3)

However, INT (formula) is the integer part [0017] of the value of a formula. Here, since the multiplier of the FIR filter 102 is designed so that the gain of a passband may be set to 0dB when 256 time-izing, when the input sampling frequency Fs1 is larger than the output sampling frequency Fs2, it performs a gain adjustment as shown in the value calculated by filter count by the degree type (4).

[0018] $z(k) = (k) \times (n/256) \dots\dots\dots (4)$

However, $z(k)$ is the calculated value (interpolation data) of an FIR filter.

[0019] As the interpolation data outputted from the FIR filter 102 are inputted into the linear interpolation means 103 and it is shown by drawing 4, linear interpolation is carried out from the data of the both ends of an output digital signal sample location using the multiplier value alpha defined by the I/O sample frequency ratio tau, and the result is outputted. In addition, count of these single strings and the output of sampled value are performed to the timing of the 2nd sampling frequency.

[0020] Thus, according to the 1st example of the above, since the value for two points of arbitration is calculated by the linear interpolation means 103, the multiplier of the FIR filter 102 can be fixed only to one, therefore it has the effectiveness that conversion between the I/O sampling frequencies of arbitration can be performed.

[0021] Drawing 2 shows the configuration of the 2nd example of this invention. This 2nd example adds the I/O sampling-frequency ratio measurement means 204 to the same input digital signal storage means 201 as the 1st example of the above, the FIR filter 202, and the linear interpolation means 203. By measuring and updating an I/O sampling-frequency ratio with this I/O sampling-frequency ratio measurement means 204 from the input sampling frequency and output sampling frequency which were memorized by the input digital signal storage means 201, in the 1st example of the above, it asks beforehand, and the I/O sampling-frequency ratio tau which was a fixed value can be frequently updated now in this 2nd example.

[0022] Thus, since the I/O sampling-frequency ratio tau can be updated based on the input sampling frequency memorized by the input digital signal storage means 201 according to the 2nd example of the above, it has the advantage that asynchronous association of I/O is attained.

[0023] In addition, although each above-mentioned example explained that it was asking for all interpolation data with the FIR filters 102 and 202, the actually calculated data are good only by the data of two points of the output sampled value both ends used with the linear interpolation means 103 and 203 of the next step. In this case, the whole amount of operations can be reduced sharply, and since it becomes possible to increase and calculate the tap length of that part and the FIR filters 102 and 202, it has the effectiveness that precision, such as a S/N ratio, can be raised further.

[0024]

[Effect of the Invention] Since this invention can fix the multiplier of a digital low pass filter only to one regardless of the combination of an I/O sampling frequency so that

clearly from the above-mentioned example, it has the effectiveness that conversion between the sampling frequencies of arbitration can be performed. Moreover, even when the timing of an I/O sampling frequency is asynchronous since the input digital signal storage means is preparing the input digital signal only in the part required for count of a digital low pass filter even if it updates an I/O sampling-frequency ratio frequently and an I/O sampling-frequency ratio is updated, it has the advantage that a generator lock becomes possible.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] The outline block diagram of the sampling-frequency inverter in the 1st example of this invention

[Drawing 2] The outline block diagram of the sampling-frequency inverter in the 2nd example of this invention

[Drawing 3] The mimetic diagram showing an example by the ring buffer of an input digital signal storage means

[Drawing 4] The time amount wave form chart for linear interpolation means explanation

[Drawing 5] The outline block diagram of the conventional sampling-frequency inverter

[Description of Notations]

101 Input Digital Signal Storage Means

102 FIR Filter (Digital Low Pass Filter)

103 Linear Interpolation Means

201 Input Digital Signal Storage Means

202 FIR Filter (Digital Low Pass Filter)

203 Linear Interpolation Means

204 I/O Sampling-Frequency Ratio Measurement Means
